CLAIMS

What is claimed is:

1. A method for analyzing a circuit design, comprising:

detecting access to at least one block of the circuit design;

if the one block is not loaded within a circuit model of computer memory, determining whether loading the one block into the circuit model would exceed a predefined maximum utilization of the computer memory;

if loading the one block into the circuit model would exceed the predefined maximum utilization, unloading one or more blocks from the circuit model and loading the one block into the circuit model;

if loading the one block into the circuit model would not exceed the predefined maximum utilization, loading the one block into the circuit model.

2. The method of claim 1, further comprising updating a block access table to record the access to the one block, if the one block is loaded within the circuit model;

wherein the steps of updating and loading comprise recording the access to the block in the block access table; and

wherein the step of unloading comprises utilizing the block access table to determine which blocks to unload from the circuit model.

3. The method of claim 2, the step of unloading further comprising utilizing an LRU caching technique with information of the block access table to determine which blocks to unload.

4. The method of claim 2, the step of unloading further comprising utilizing an LFU caching technique with information of the block access table to determine which blocks to unload.

5. A system for analyzing a circuit design, comprising:

computer memory for storing a circuit model of the circuit design;

an analysis tool for analyzing the circuit design by accessing one or more blocks of the circuit model; and

a model manager for (a) loading one or more blocks of the circuit design to the circuit model and (b) unloading one or more blocks from the circuit model such that the circuit model does not exceed a predefined maximum utilization of the computer memory.

6. The system of claim 5, further comprising a storage unit for storing the circuit design.

7. The system of claim 5, further comprising a block access table for recording access to blocks of the circuit model by the analysis tool.

8. The system of claim 7, the model manager being operable to determine which blocks to remove from the circuit model by utilizing information of the block access table.

9. The system of claim 8, the model manager employing an LRU caching technique with information of the block access table to determine which blocks to remove from the circuit model.

10. The system of claim 8, the model manager employing an LFU caching technique with information of the block access table to determine which blocks to remove from the circuit model.

11. A system for analyzing a circuit design, comprising:

means for detecting access to at least one block of the circuit design;

means for determining whether loading the one block into a circuit model, stored within computer memory, would exceed a predefined maximum utilization of the computer memory when the one block is not currently within the circuit model;

means for unloading one or more blocks from the circuit model and loading the one block into the circuit model when loading the one block into

computer memory would exceed the predefined maximum utilization; and

means for loading the one block into the circuit model when loading the one block into the computer model would not exceed the predefined maximum utilization.

12. The system of claim 11, further comprising means for recording the block access.

13. The system of claim 12, wherein the means for recording records the block access in a block access table.

14. The system of claim 13, further comprising means for utilizing the block access table to determine which blocks to unload from the circuit model.

15. The system of claim 14, the means for utilizing further comprising means for utilizing an LRU caching technique to determine which blocks to unload from the circuit model.

16. The system of claim 14, the means for utilizing further comprising means for utilizing an LFU caching technique to determine which blocks to unload from the circuit model.

17. A software product comprising instructions, stored on computer-readable media, wherein the instructions, when executed by a computer, perform steps for analyzing a circuit design with reduced memory utilization, comprising:

instructions for detecting access to at least one block of the circuit design;

instructions for recording the access when the one block is loaded within a circuit model of computer memory;

instructions for determining whether loading the one block into the circuit model would exceed a predefined maximum utilization of the computer memory, when the one block is not loaded within the circuit model;

instructions for unloading one or more blocks from the circuit model and loading the one block into the circuit model, when loading the one

block into the circuit model would exceed the predefined maximum utilization; and

instructions for loading the one block into the circuit model, when loading the one block into the circuit model would not exceed the predefined maximum utilization.

18. The software product of claim 17, further comprising instructions for recording the access in a block access table.

19. The software product of claim 18, further comprising instructions for utilizing the block access table to determine which blocks to unload.

20. The software product of claim 19, further comprising instructions for utilizing an LRU caching technique to determine which blocks to unload.

21. The software product of claim 19, further comprising instructions for utilizing an LFU caching technique to determine which blocks to unload.

22. The software product of claim 17, further comprising instructions for setting the predefined maximum utilization.